晶采光電科技股份有限公司
AMPIRE CO., LTD.

SPECIFICATIONS FOR LCD MODULE

CUSTOMER	
CUSTOMER PART NO.	
AMPIRE PART NO.	AM-320240LGTMQW-T00H
APPROVED BY	
DATE	

☐ Approved For Specifications
☑ Approved For Specifications & Sample

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RECORD OF REVISION

Revision Date	Page	Contents	Editor
2012/8/16	--	New Release	Leo
2012/10/09	24	Add the initial code	Leo

1 Features

3.5 inch Amorphous-TFT-LCD (Thin Film Transistor Liquid Crystal Display) module. This module is composed of a 3.5" TFT-LCD panel, LCD controller and White LED Backlight unit.

1.1 TFT Panel Feature :

(1) Construction: 3.5" a-Si color TFT-LCD, White LED Backlight and Touch Panel.

(2) Resolution (pixel): 320(R.G.B) X240

(3) Number of the Colors : 262K/65K colors.

(4) LCD type : Transmissive ,TFT LCD (normally White)

(5) Interface: 8/9/16/18bits 6800series/8080series,Serial&RGB Interface

(6) Power Supply Voltage: 3.3V single power input. Built-in power supply circuit.

2 Physical specifications

Item	Specifications	Unit
Display resolution(dot)	320x3(W) x 240(H)	dot
Active area	70.08 (W) x 52.56 (H)	mm
Screen size	3.5(Diagonal)	mm
Pixel size	0.073 (W) x 0.219 (H)	mm
Color configuration	R.G.B stripe	
View direction (Gray inversion)	6 o'clock	
Overall dimension	77.8(W)x129.5(H) x4.3(D)	mm
Weight	42	g
Backlight unit	LED	

3 Electrical specification

3.1 Absolute max. ratings

3.1.1 Electrical Absolute max. ratings

Item	Symbol	Condition	Min.	Max.	Unit	Remark
Power voltage	VDD	VSS=0	-0.3	5.0	V	
Input voltege	V_{in}		-0.3	VDD+0.3	V	Note 1

Note1: /CS,/WR,/RD,RS,DB0~DN17

3.1.2 Environmental Absolute max. ratings

Item	OPERATING		STORAGE		Remark
	MIN	MAX	MIN	MAX	
Temperature	-20	70	-30	80	Note2,3,4,5,6,7
Humidity	Note1		Note1		
Corrosive Gas	Not Acceptable		Not Acceptable		

Note1 : Ta <= 40℃ : 85% RH max

Ta > 40℃ : Absolute humidity must be lower than the humidity of 85%RH at 40℃

Note2 : For storage condition Ta at -30℃ < 48h , at 80℃ < 100h

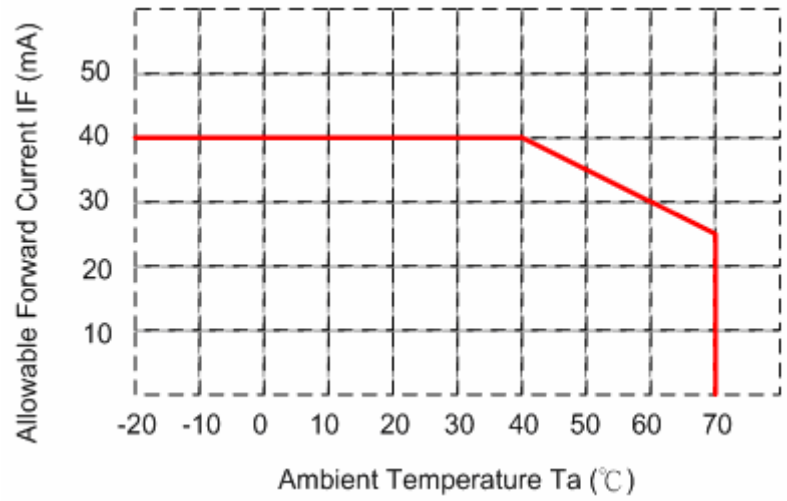
For operating condition Ta at -20℃ < 100h

Note3 : Background color changes slightly depending on ambient temperature. This phenomenon is reversible.

Note4 : The response time will be slower at low temperature.

Note5 : Only operation is guarantied at operating temperature. Contrast, response time, another display quality are evaluated at +25℃

Note6 : When LCM is operated over 40℃ ambient temperature, the I_{LED} of the LED back-light should be follow :



Note7 : This is panel surface temperature, not ambient temperature.

Note8 : When LCM be operated over than 40℃, the life time of the LED back-light will be reduced.

3.1.3 LED back-light Unit Absolute max. ratings

Item	Symbol	Ratings	Unit	Remark
Peak forward Current	IF	60	mA	
Reverse Voltage	VR	15	V	
Power Dissipation	Po	0.9	W	

3.2 Electrical characteristics

3.2.1 DC Electrical characteristic of the LCD

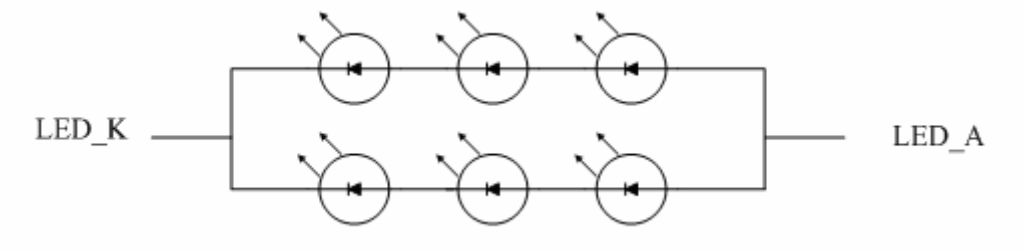
Typical operating conditions (VSS=0V)

Item		Symbol	Min.	Typ.	Max.	Unit	Remark
Power supply		VDD	2.5	3.3	3.6	V	
Input Voltage for logic	H Level	V_{IH}	0.8VDD	-	VDD	V	
	L Level	V_{IL}	0	-	0.2VDD	V	
Output Voltage for Logic	H Level	V_{OH}	0.9 VDD	-	VDD	V	
	L Level	V_{OL}	0		0.1 VDD	V	
Power Supply current		IDD	-	9.1	-	mA	*Note

*Note: f_V =60Hz, Ta=25℃, Display pattern: All Black

3.2.2 Electrical characteristic of LED Back-light

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
LED voltage	V_{AK}	--	9.6	11.0	V	I_{LED} =40,Ta=25℃
LED forward current	I_{LED}	--	40	--	mA	Ta=25℃
	I_{LED}	--	30	--	mA	Ta=60℃
Lamp life time		--	10K	--	Hr	I_{LED} =40,Ta=25℃

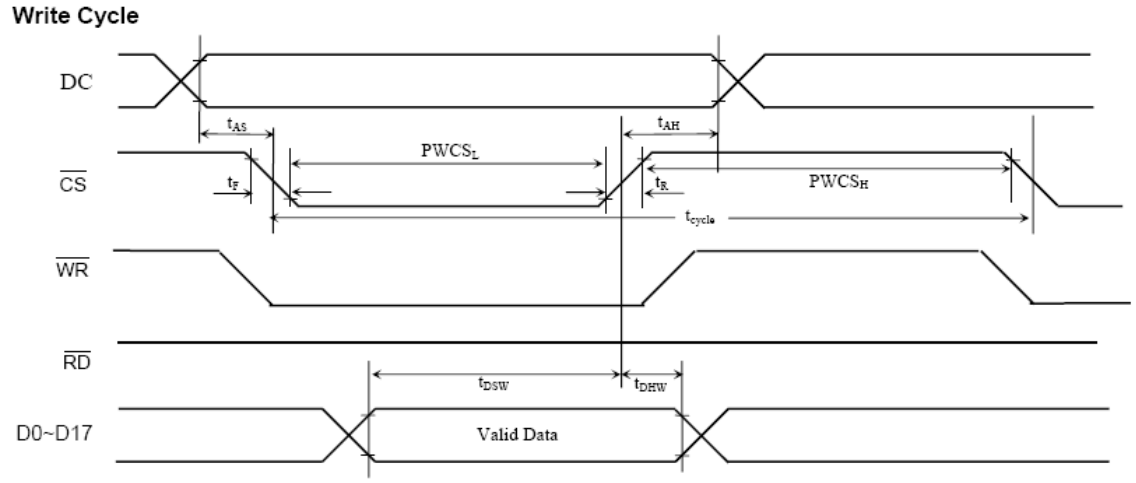


■ The constant current source is needed for white LED back-light driving.

When LCM is operated over 60℃ ambient temperature, the I_{LED} of the LED back-light should be adjusted to 30mA max.

3.3 AC Timing characteristic of the TFT LCD controller

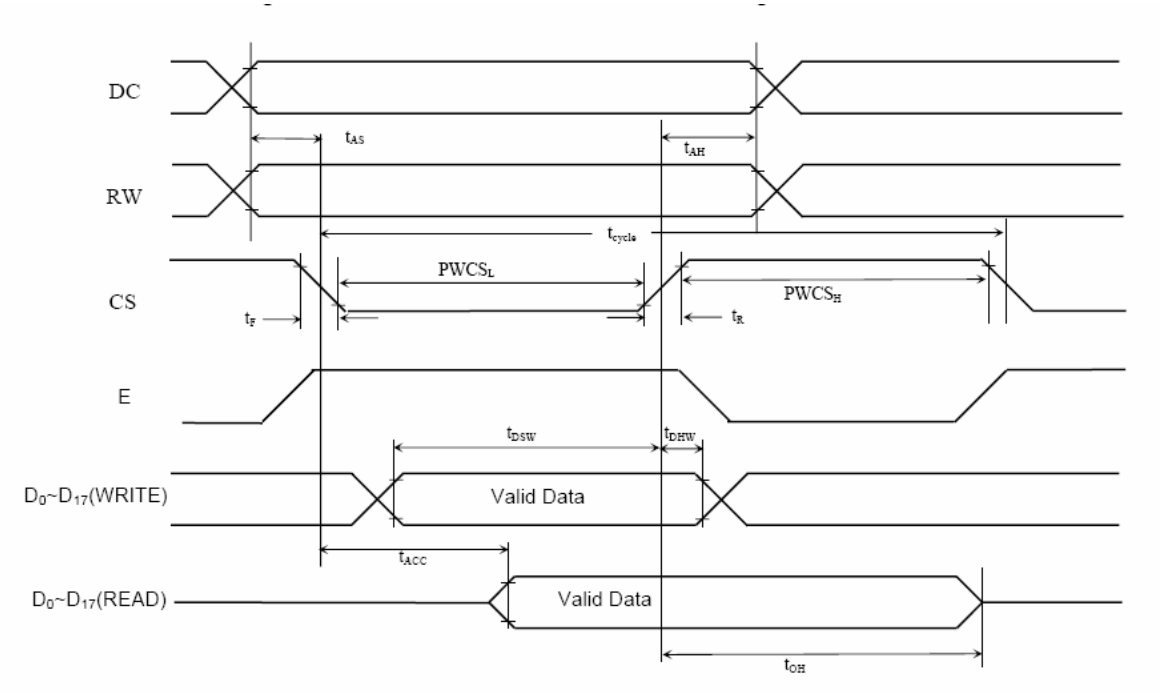
3.3.1 Parallel 8080 Timing Characteristics



(Ta = -20℃~70℃ VDDIO=1.65~3.6V)

Symbol	Parameter	Min	Typ	Max	Unit	Remark
t_{cycle}	Clock cycle time(write cycle)	100	-	-	ns	
t_{cycle}	Clock cycle time(Read cycle)	1000	-	-	ns	
t_{AS}	Address setup time	0	-	-	ns	
t_{AH}	Address hold time	0	-	-	ns	
t_{DSW}	Data Setup time	5	-	-	ns	
t_{DHW}	Data Hold time	5	-	-	ns	
t_{ACC}	Data Access time	250	-	-	ns	
t_{OH}	Output Hold time	100	-	-	ns	
$PWCS_L$	Pulse Width /CS low(write cycle)	50	-	-	ns	
$PWCS_H$	Pulse Width /CS High(write cycle)	50	-	-	ns	
$PWCS_L$	Pulse Width /CS low(read cycle)	500	-	-	ns	
$PWCS_H$	Pulse Width /CS High(read cycle)	500	-	-	ns	
t_R	Rise time	-	-	4	ns	
t_F	Fall time	-	-	4	ns	

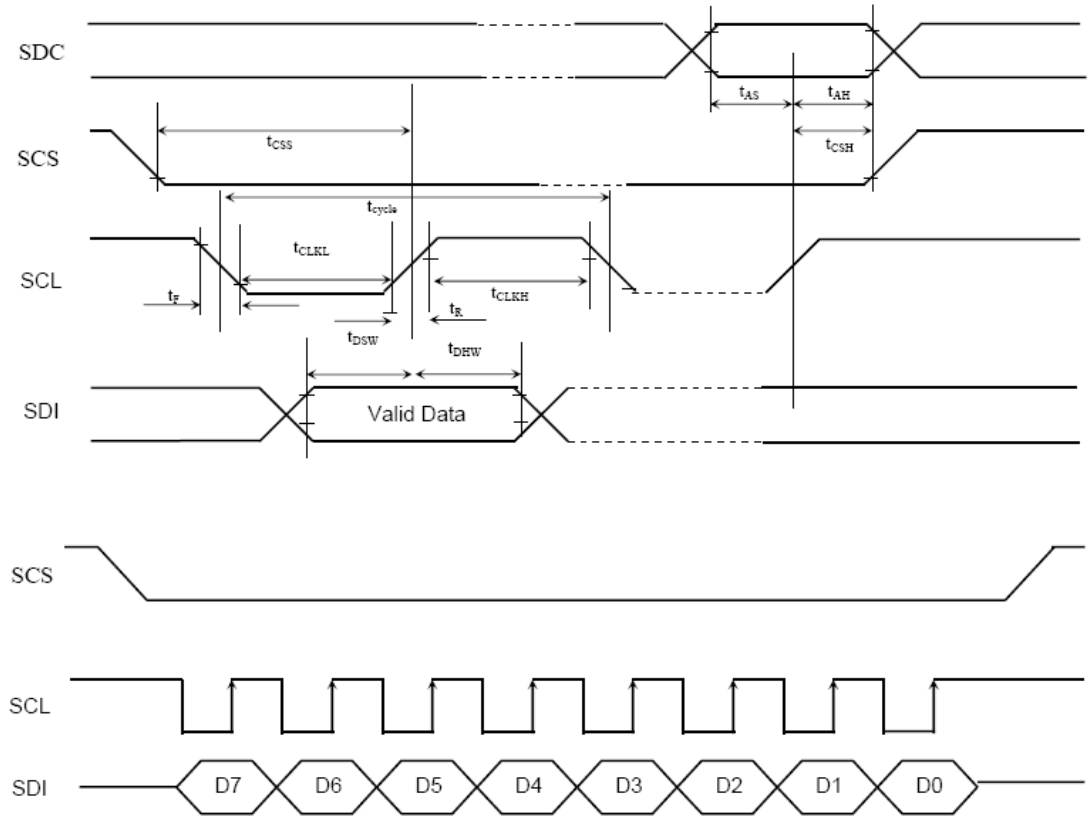
3.3.2 Parallel 6800 Timing Characteristics



(Ta = -20℃~70℃ VDDIO=1.65~3.6V)

Symbol	Parameter	Min	Typ	Max	Unit	Remark
t_{cycle}	Clock cycle time(write cycle)	100	-	-	ns	
t_{cycle}	Clock cycle time(Read cycle)	1000	-	-	ns	
t_{AS}	Address setup time	0	-	-	ns	
t_{AH}	Address hold time	0	-	-	ns	
t_{DSW}	Data Setup time	5	-	-	ns	
t_{DHW}	Data Hold time	5	-	-	ns	
t_{ACC}	Data Access time	250	-	-	ns	
t_{OH}	Output Hold time	100	-	-	ns	
$PWCS_L$	Pulse Width /CS low(write cycle)	50	-	-	ns	
$PWCS_H$	Pulse Width /CS High(write cycle)	50	-	-	ns	
$PWCS_L$	Pulse Width /CS low(read cycle)	500	-	-	ns	
$PWCS_H$	Pulse Width /CS High(read cycle)	500	-	-	ns	
t_R	Rise time	-	-	4	ns	
t_F	Fall time	-	-	4	ns	

3.3.3 Serial Timing Characteristics

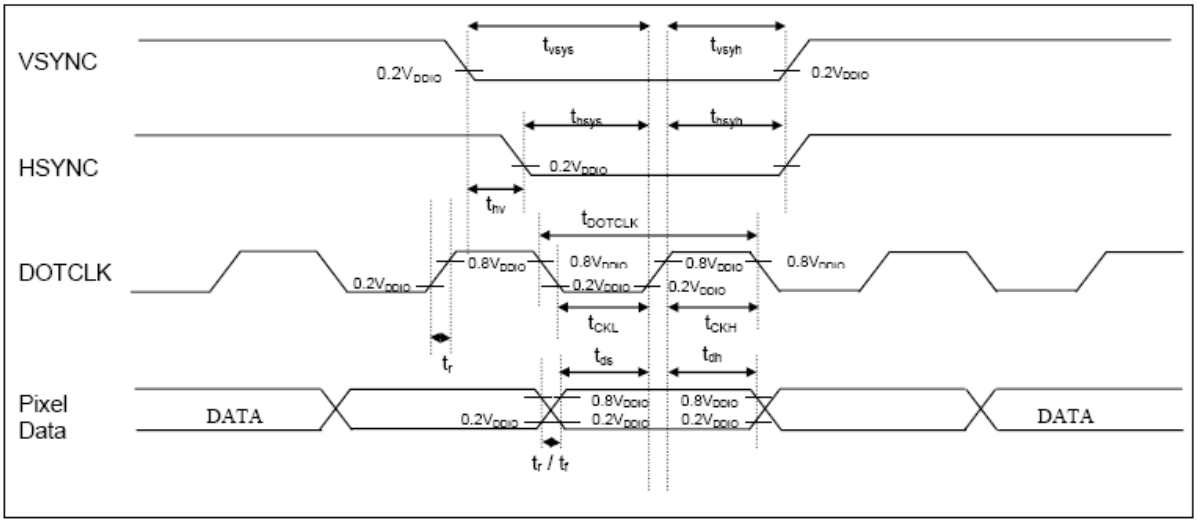


(Ta = -20℃~70℃ VDDIO=1.65~3.6V)

Symbol	Parameter	Min	Typ	Max	Unit	Remark
t_{cycle}	Clock cycle time	77	-	-	ns	
f_{CLK}	Serial Clock cycle time SPI Clock tolerance = +/- 2ppm	-	-	13	MHz	
t_{AS}	Address setup time	4	-	-	ns	
t_{AH}	Address hold time	5	-	-	ns	
t_{CSS}	Chip Select Setup time	2	-	-	ns	
t_{CSH}	Chip Select Hold time	10	-	-	ns	
t_{DSW}	Write Data Setup time	5	-	-	ns	
t_{OHW}	Write Data Hold time	10	-	-	ns	
t_{CLKL}	Clock Low time	38	-	-	ns	
t_{CLKH}	Clock High time	38	-	-	ns	
t_R	Rise time	-	-	4	ns	
t_F	Fall time	-	-	4	ns	

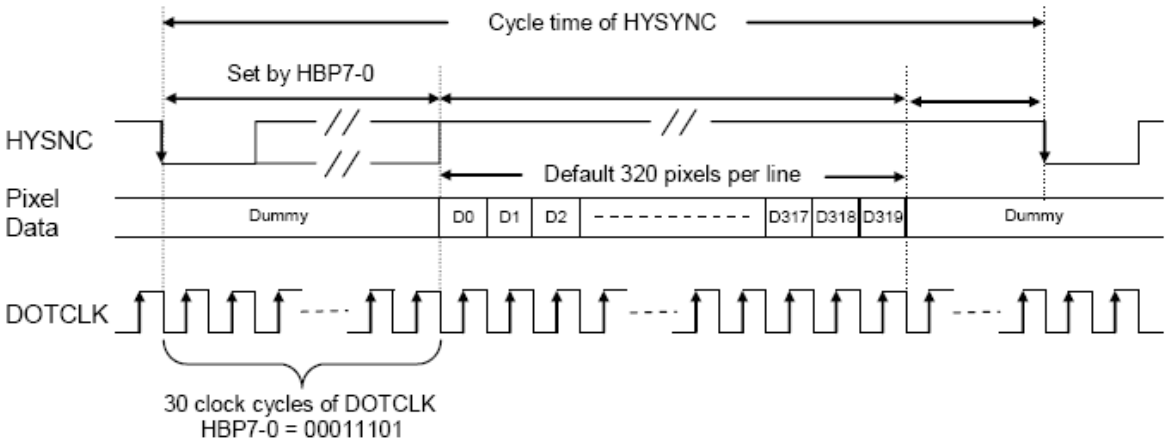
3.3.4 RGB Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
f_{DOTCLK}	DOTCLK Frequency (70Hz frame rate)	1	5.5	8.2	MHz
t_{DOTCLK}	DOTCLK Period	122	182	1000	ns
t_{VSYS}	Vertical Sync Setup Time	20	-	-	ns
t_{VSYH}	Vertical Sync Hold Time	20	-	-	ns
t_{HSYS}	Horizontal Sync Setup Time	20	-	-	ns
t_{HSYH}	Horizontal Sync Hold Time	20	-	-	ns
t_{HV}	Phase difference of Sync Signal Falling Edge	0	-	320	t_{DOTCLK}
t_{CLK}	DOTCLK Low Period	61	-	-	ns
t_{CKH}	DOTCLK High Period	61	-	-	ns
t_{DS}	Data Setup Time	25	-	-	ns
t_{DH}	Data hold Time	25	-	-	ns



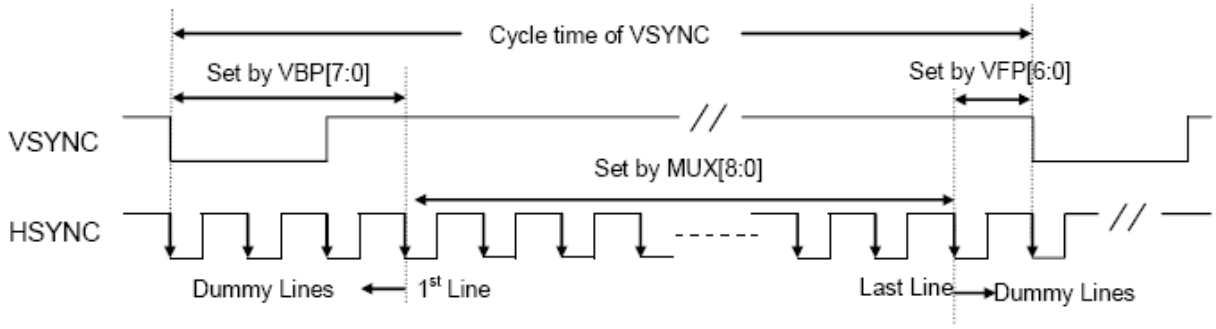
Horizontal Front Porch = 0~320 tDOTCLK

Horizontal Back Porch = 30 tDOTCLK

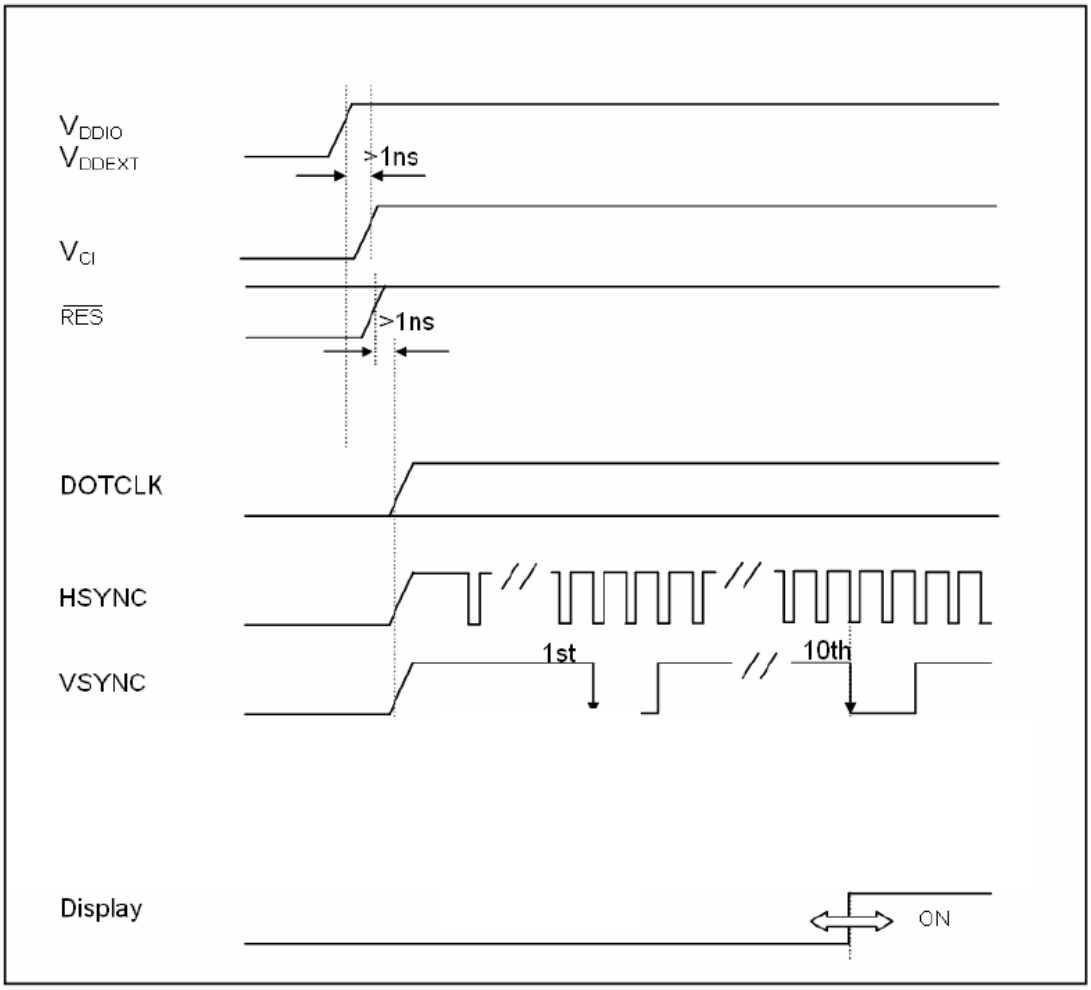


Vertical Back Porch = 4 tDOTCLK

Vertical Front Porch = 1 tDOTCLK



Power Up Sequence for RGB mode



4 Optical specification

4.1 Optical characteristic:

Item		Symbol	Conditon	Min.	Typ.	Max.	Unit	Remark
Response Time	Rise+ Fall	T_r+T_f	Θ=0°		35	50	ms	Note 1,2,3,5
Contrast ratio		CR	At optimized viewing angle	150	300	-		Note 1,2,4,5
Viewing Angle	Top Bottom Left Right		CR≧10	- - - -	50 70 70 70	- - - -	deg.	Note1,2, 5,6
Brightness LED BL		Y_L	I_{LED}=40mA ,25℃	179	224	-	cd/m^2	Note 7
White chromaticity		Xw		0.26	--	0.34		
		Yw		0.27	--	0.35		

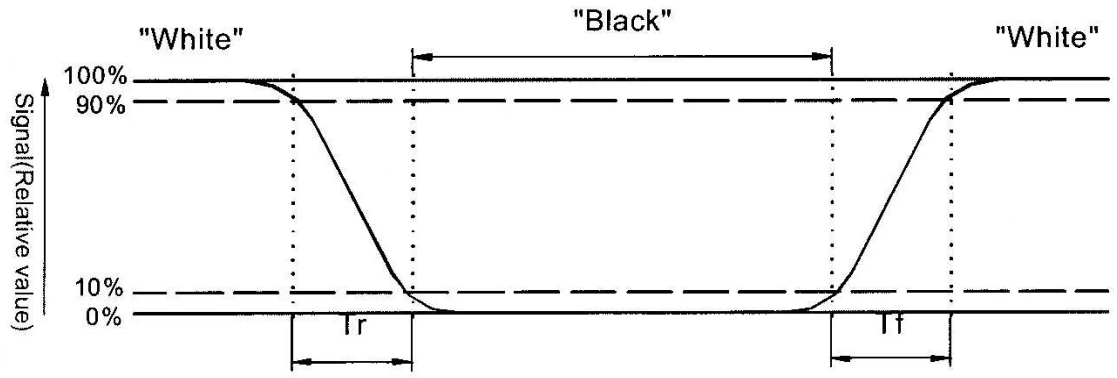
( ) For reference only. These data should be update according the prototype.

Note 1: Ambient temperature=25℃, and lamp current I_{LED}=40mA.To be measured in the dark room.

Note 2:To be measured on the center area of panel with a viewing cone of 1°by Topcon luminance meter BM-7,after 10 minutes operation.

Note 3.Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “black“ to “white”(falling time) and from “white” to “black” (rising time),respectively. The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.



Note 4.Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at "White" state}}{\text{Photo detector Output when LCD is at "Black" state}}$$

Note 5.White $V_i = V_{i50} + 1.5V$

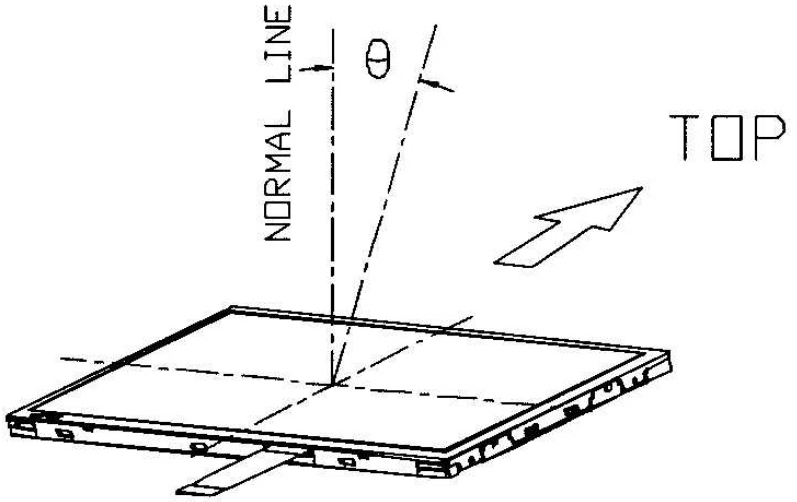
Black $V_i = V_{i50} + 2.0V$

"±"means that the analog input signal swings in phase with V_{COM} signal.

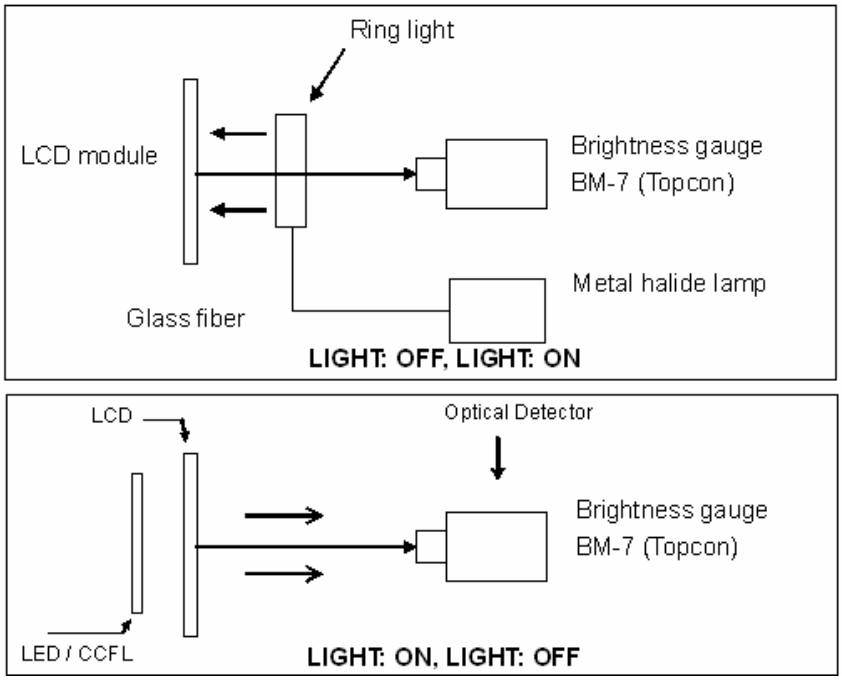
"$\overset{-}{+}$" means that the analog input signal swings out of phase with V_{COM} signal.

V_{i50} : The analog input voltage when transmission is 50%.The 100% Transmission is defined as the transmission of LCD panel when all the Input terminals of module are electrically opened.

Note 6.Definition of viewing angle, Refer to figure as below.



Note 7.Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.



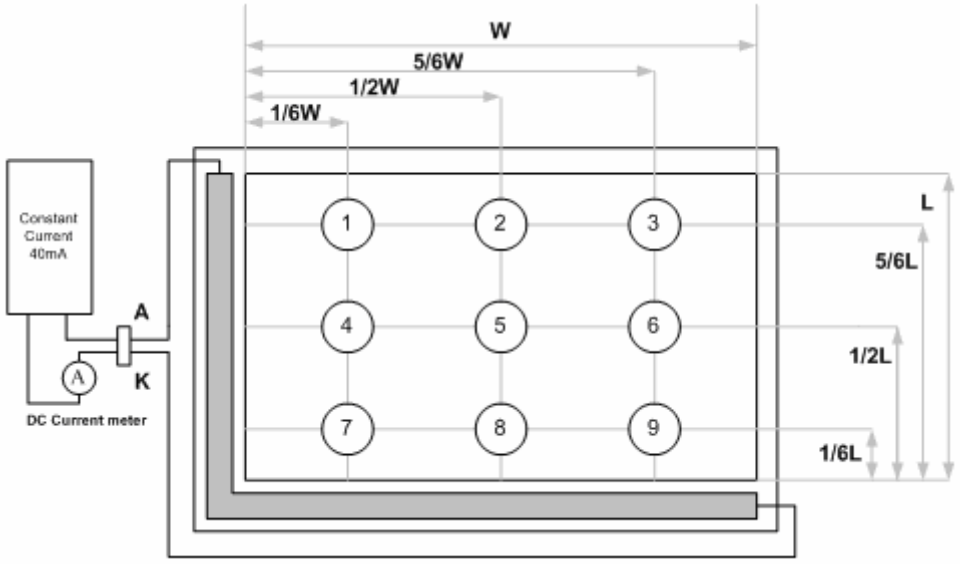
4.2 Optical characteristic of the LED Back-light

ITEM	MIN	TYP	MAX	UNIT	Condition
Bare Brightness	2800	--	--	Cd/m^2	I_{LED} =40mA,Ta=25℃
AVG. X of 1931 C.I.E.	0.26	0.30	0.34	--	I_{LED} =40mA,Ta=25℃
AVG. Y of 1931 C.I.E.	0.27	0.31	0.35	--	I_{LED} =40mA,Ta=25℃
Brightness Uniformity	75	--	--	%	I_{LED} =40mA,Ta=25℃

( )For reference only. These data should be update according the prototype.

Note1 : Measurement after 10 minutes from LED BL operating.

Note2 : Measurement of the following 9 places on the display.



Note3: The Uniformity definition

(Min Brightness / Max Brightness) x 100%

4.3 Touch Panel Electrical Specification

Parameter	Condition	Standard Value
Terminal Resistance	X Axis	400 ~ 900 Ω
	Y Axis	200 ~ 500 Ω
Insulating Resistance	DC 25 V	More than 10MΩ
Linearity	--	±1.5 %
Notes life by Pen	Note a	100,000 times(min)
Input life by finger	Note b	1,000,000 times (min)

Note A.

Notes area for pen notes life test is 10 x 9 mm.

Size of word is 7.5 x 6.72

Shape of pen end: R0.8

Load: 250 g

Note B

By Silicon rubber tapping at same point

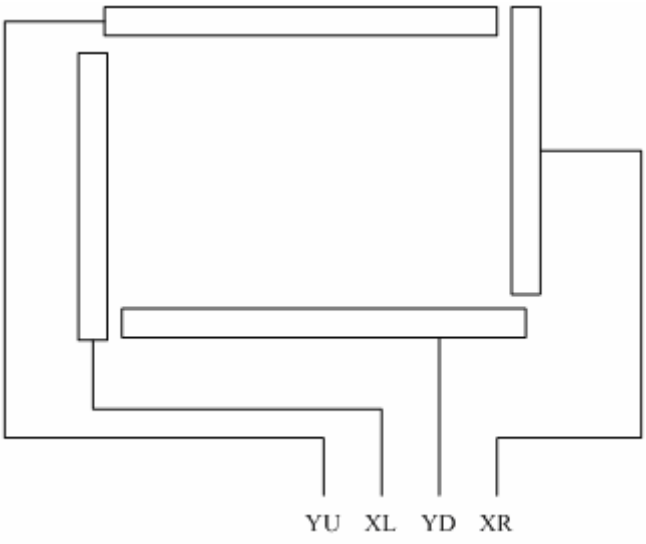
Shape of rubber end: R8

Load: 200g

Frequency: 5 Hz

Interface

No.	Symbol	Function
1	XR	Touch Panel Right Signal in X Axis
2	YU	Touch Panel Upper Signal in Y Axis
3	XL	Touch Panel Left Signal in X Axis
4	YD	Touch Panel Low Signal in Y Axis



5 Interface specifications

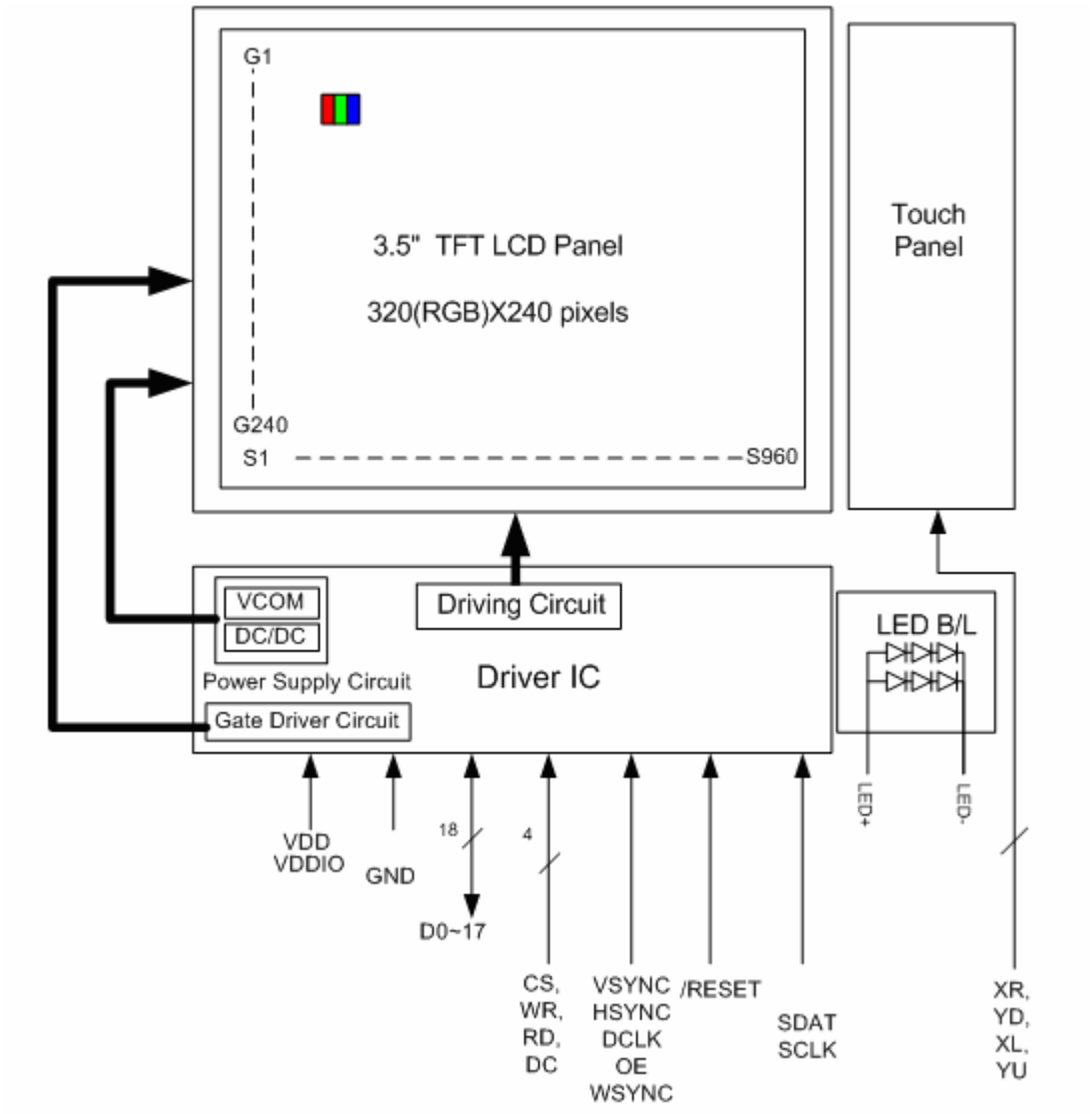
Pin no	Symbol	I/O	Description	Remark
1	LED-	I	Backlight LED	
2	LED-	I	Backlight LED	
3	LED+	I	Backlight LED	
4	LED+	I	Backlight LED	
5	NC	-	No Connection.	
6	/RESET	I	Reset signal for TFT LCD controller.	
7	NC	-	No Connection.	
8	XR	-	Touch Panel Right Signal in X Axis.	
9	YD	-	Touch Panel Down Signal in Y Axis.	
10	XL	-	Touch Panel Left Signal in X Axis.	
11	YU	-	Touch Panel Up Signal in Y Axis.	
12	NC	-	No Connection.	
13	DC/SDC	I	Register and Data select for TFT LCD controller. SDC: Serial interface	
14	RD	I	80mode: /RD low active signal for TFT LCD controller. 68mode: R/W signal Hi: read, Lo: write.	
15	WR	I	80mode: /WR low active signal for TFT LCD controller. 68mode: E signal latch on rising edge.	
16	CS/SCS	I	Chip select low active signal for TFT LCD controller. SCS: Chip Select pin for Serial interface	
17	WSYNC	O	Ram Write Synchronization output	
18	D17	I	Data Bus (D0 ~ D17)	
19	D16	I		
20	D15	I		
21	D14	I		
22	D13	I		
23	D12	I		
24	D11	I		
25	D10	I		
26	D9	I		
27	D8	I		
28	D7	I		
29	D6	I		
30	D5	I		
31	D4	I		
32	D3	I		
33	D2	I		
34	D1	I		
35	D0	I		
36	HSYNC	I	Horizontal Sync Input	
37	VSYNC	I	Vertical Sync Input	
38	DCLK	I	Dot Data Clock	
39	NC	-	No Connection.	
40	NC	-	No Connection.	
41	VDD	I	Power supply for the logic (3.3V).	

42	VDD	I	Power supply for the logic (3.3V).	
43	NC	-	No Connection.	
44	PS0	I	Interface Selection	Note*
45	NC	-	No Connection.	
46	PS1	I	Interface Selection	Note*
47	NC	-	No Connection.	
48	PS2	I	Interface Selection	Note*
49	SCLK	I	Serial clock input	
50	SDAT	I	Serial Data input	
51	PS3	I	Interface Selection	Note*
52	OE	I	Data Enable Input	
53	GND	I	Ground	
54	GND	I	Ground	

Note*:

PS3	PS2	PS1	PS0	Interface Mode
0	0	0	0	16-bit 6800 parallel interface
0	0	0	1	8-bit 6800 parallel interface
0	0	1	0	16-bit 8080 parallel interface
0	0	1	1	8-bit 8080 parallel interface
0	1	0	0	9-bit generic D[8:0] (262k colour) + 3-wire SPI If 65K color, D3 shorts to D8 internally
0	1	0	1	16-bit generic (262k colour) + 3-wire SPI
0	1	1	0	18-bit generic (262k colour) + 3-wire SPI
0	1	1	1	6-bit generic D[8:3] (262k colour) + 3-wire SPI
1	0	0	0	18-bits 6800 parallel interface
1	0	0	1	9-bits 6800 parallel interface
1	0	1	0	18-bit 8080 parallel interface
1	0	1	1	9-bit 8080 parallel interface
1	1	1	0	3-wire SPI
1	1	1	1	4-wire SPI

6 BLOCK DIAGRAM



7 Interface Protocol

7.1 Interface Setting

PS3	PS2	PS1	PS0	Interface Mode
0	0	0	0	16-bit 6800 parallel interface
0	0	0	1	8-bit 6800 parallel interface
0	0	1	0	16-bit 8080 parallel interface
0	0	1	1	8-bit 8080 parallel interface
0	1	0	0	9-bit generic D[8:0] (262k colour) + 3-wire SPI If 65K color, D3 shorts to D8 internally
0	1	0	1	16-bit generic (262k colour) + 3-wire SPI
0	1	1	0	18-bit generic (262k colour) + 3-wire SPI
0	1	1	1	6-bit generic D[8:3] (262k colour) + 3-wire SPI
1	0	0	0	18-bits 6800 parallel interface
1	0	0	1	9-bits 6800 parallel interface
1	0	1	0	18-bit 8080 parallel interface
1	0	1	1	9-bit 8080 parallel interface
1	1	1	0	3-wire SPI
1	1	1	1	4-wire SPI

7.1.1 6800-series System Bus Interface

PS3	PS2	PS1	PS0	Interface Mode	Data bus	RW	E	DC	/CS	Operation
0	0	0	0	16-bit 6800 parallel interface	D[17:10], D[8:1]	1	↴	0	0	Read 8-bit command
						1	↴	1	0	Read 8-bit parameters or status*
						0	↴	0	0	Write 8-bit command
						0	↴	1	0	Write 16-bit display data
0	0	0	1	8-bit 6800 parallel interface	D[8:1]	1	↴	0	0	Read 8-bit command
						1	↴	1	0	Read 8-bit parameters or status*
						0	↴	0	0	Write 8-bit command
						0	↴	1	0	Write 8-bit display data
1	0	0	0	18-bits 6800 parallel interface	D[17:0]	1	↴	0	0	Read 8-bit command
						1	↴	1	0	Read 8-bit parameters or status*
						0	↴	0	0	Write 8-bit command
						0	↴	1	0	Write 18-bit display data
1	0	0	1	9-bits 6800 parallel interface	D[8:0]	1	↴	0	0	Read 8-bit command
						1	↴	1	0	Read 8-bit parameters or status*
						0	↴	0	0	Write 8-bit command
						0	↴	1	0	Write 9-bit display data

* A dummy read is required before the first actual display data read

7.1.2 8080-series System Bus Interface

PS3	PS2	PS1	PS0	Interface Mode	Data bus	/WR	/RD	DC	/CS	Operation
0	0	1	0	16-bit 8080 parallel interface		1	0	0	0	Read 8-bit command
						1	0	1	0	Read 8-bit parameters or status*
						0	1	0	0	Write 8-bit command
						0	1	1	0	Write 16-bit display data
0	0	1	1	8-bit 8080 parallel interface		1	0	0	0	Read 8-bit command
						1	0	1	0	Read 8-bit parameters or status*
						0	1	0	0	Write 8-bit command
						0	1	1	0	Write 8-bit display data
1	0	1	0	18-bit 8080 parallel interface		0	1	0	0	Read 8-bit command
						1	0	1	0	Read 8-bit parameters or status*
						0	1	0	0	Write 8-bit command
						0	1	1	0	Write 18-bit display data
1	0	1	1	9-bit 8080 parallel interface		1	0	0	0	Read 8-bit command
						1	0	1	0	Read 8-bit parameters or status*
						0	1	0	0	Write 8-bit command
						0	1	1	0	Write 9-bit display data

* A dummy read is required before the first actual display data read

7.2 Mapping for Writing an Instruction

		Hardware pins																	
Interface	Cycle	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
18 bits		IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	x	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0	x
16 bits		IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8		IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0	
9 bits	1st	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	x									
	2nd	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0	x									
8 bits	1st	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8										
	2nd	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0										

Remark : x Don't care bits
Not connected pins

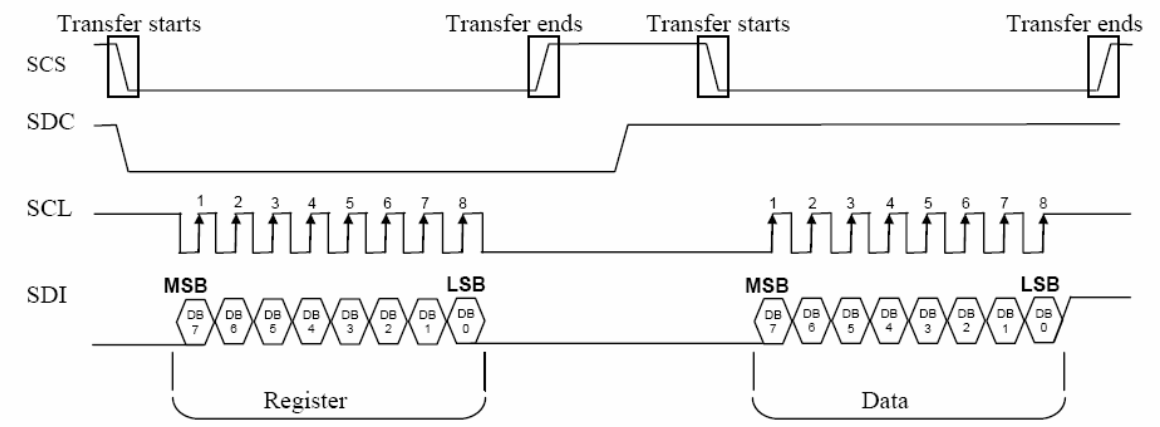
7.3 Mapping for Writing Pixel Data

			Hardware pins																	
Interface	Color mode	Cycle	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
18 bits	262k		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
16 bits	262k	1st	R5	R4	R3	R2	R1	R0	x	x		G5	G4	G3	G2	G1	G0	x	x	
		2nd	B5	B4	B3	B2	B1	B0	x	x		R5	R4	R3	R2	R1	R0	x	x	
		3rd	G5	G4	G3	G2	G1	G0	x	x		B5	B4	B3	B2	B1	B0	x	x	
		1st	R5	R4	R3	R2	R1	R0	x	x		G5	G4	G3	G2	G1	G0	x	x	
		2nd	x	x	x	x	x	x	x	x		B5	B4	B3	B2	B1	B0	x	x	
		1st	R5	R4	R3	R2	R1	R0	x	x		G5	G4	G3	G2	G1	G0	x	x	
		2nd	B5	B4	B3	B2	B1	B0	x	x		x	x	x	x	x	x	x	x	
	65k		R4	R3	R2	R1	R0	G5	G4	G3		G2	G1	G0	B4	B3	B2	B1	B0	
9 bits	262k	1st	R5	R4	R3	R2	R1	R0	G5	G4	G3									
		2nd	G2	G1	G0	B5	B4	B3	B2	B1	B0									
8 bits	262k	1st	R5	R4	R3	R2	R1	R0	x	x										
		2nd	G5	G4	G3	G2	G1	G0	x	x										
		3rd	B5	B4	B3	B2	B1	B0	x	x										
	65k	1st	R4	R3	R2	R1	R0	G5	G4	G3										
		2nd	G2	G1	G0	B4	B3	B2	B1	B0										

Remark : x Don't care bits
Not connected pins

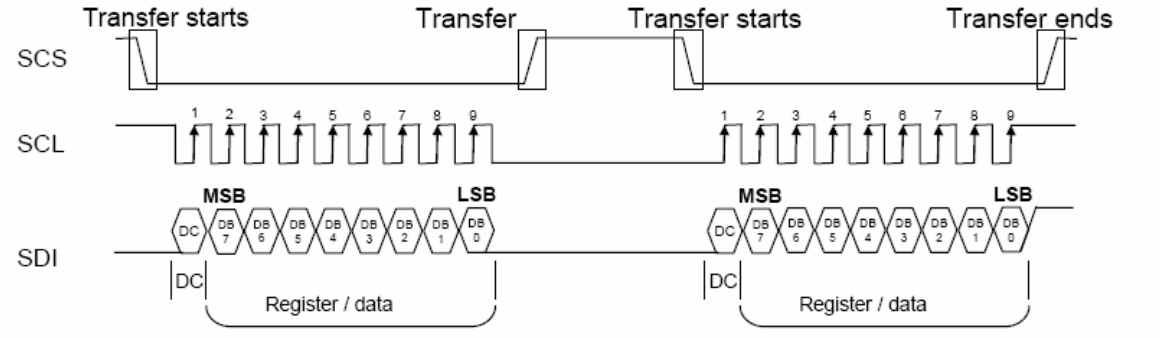
7.4 4-wire Serial Peripheral Interface (8 bits)

The clock synchronized serial peripheral interface (SPI) using the chip select line (SCS), serial transfer clock line (SCL), serial input data (SDI). The serial data transfer starts at the falling edge of SCS input and ends at the rising edge of SCS.
SDC determinates the data of SDI which is register or data.



7.5 3-wire Serial Peripheral Interface (9 bits)

The operation is similar to 4-lines serial peripheral interface while SDC is not use. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: DC bit, D7 to D0 bit. The DC bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (DC bit = 1) or the command register (DC bit = 0).



7.6 RGB Interface

RGB interface unit consists of D [17:0], HSYNC, VSYNC, DOTCLK and OE signals for display moving pictures. When the RGB interface is selected, the display operation is synchronized with external control signals (HSYNC, VSYNC and DOTCLK). Data is written in synchronization with the control signals when DEN is enabled for write operation in order to avoid flicker or tearing effect while updating display data.

7.7 Mapping for Writing Pixel Data in generic mode

Interface	Color mode	Cycle	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
18-bit RGB	262k	-	RR5	RR4	RR3	RR2	RR1	RR0	GG5	GG4	GG3	GG2	GG1	GG0	BB5	BB4	BB3	BB2	BB1	BB0
16-bit RGB	65k	-	RR5	RR4	RR3	RR2	RR1	RR4	GG5	GG4	GG3	GG2	GG1	GG0	BB4	BB3	BB2	BB1	BB0	BB4
9-bit RGB	262k	1st	RR5	RR4	RR3	RR2	RR1	RR0	GG5	GG4	GG3									
		2nd	BB5	BB4	BB3	BB2	BB1	BB0	GG2	GG1	GG0									
6-bit RGB	262k	1st	RR5	RR4	RR3	RR2	RR1	RR0												
		2nd	GG5	GG4	GG3	GG2	GG1	GG0												
		3rd	BB5	BB4	BB3	BB2	BB1	BB0												

8 Register Depiction

8.1

Reg#	Register	R/W	D/C	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R	Index	0	0	0	0	0	0	0	0	0	0	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
SR	Status Read	1	0	L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	0	0	0	0
R00h	Oscillation Start	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	OSCEN
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R01h	Driver output control	0	1	0	RL	REV	GD	BGR	SM	GS	0	MUX7	MUX6	MUX5	MUX4	MUX3	MUX2	MUX1	MUX0
	(3AEFh)			0	0	1	1	1	0	1	0	1	1	1	0	1	1	1	1
R02h	LCD drive AC control	0	1	0	0	0	FLD	ENWS	B/C	EOR	WSMD	NW7	NW6	NW5	NW4	NW3	NW2	NW1	NW0
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R03h	Power control (1)	0	1	DCT3	DCT2	DCT1	DCT0	BT2	BT1	BT0	0	DC3	DC2	DC1	DC0	AP2	AP1	AP0	0
	All GAMAS[2:0] setting 8 color (6A64h)			0	1	1	0	1	0	1	0	0	1	1	0	0	1	0	0
R07h	Display control	0	1	0	0	0	PT1	PT0	VLE2	VLE1	SPT	0	0	GON	DTE	CM	0	D1	D0
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R0Bh	Frame cycle control	0	1	NO1	NO0	SDT1	SDT0	0	EQ2	EQ1	EQ0	DIV1	DIV0	SDIV	SRTN	RTN3	RTN2	RTN1	RTN0
	(5308h)			0	1	0	1	0	0	1	1	0	0	0	0	1	0	0	0
R0Ch	Power control (2)	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	VRC2	VRC1	VRC0
	(0004h)			0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
R0Dh	Power control (3)	0	1	0	0	0	0	0	0	0	0	0	0	0	0	VRH3	VRH2	VRH1	VRH0
R0Eh	Power control (4)	0	1	0	0	VCOMG	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	0	0	0	0	0
R0Fh	Gate scan start position	0	1	0	0	0	0	0	0	0	SCN8	SCN7	SCN6	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R10h	Sleep mode	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SLP
	(0001h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R11h	Entry mode	0	1	VS mode	DFM1	DFM0	0	Denmode	WMode	Nosync	DMode	TY1	TY0	ID1	ID0	AM	0	0	0
	(6830h)			0	1	1	0	0	1	1	0	0	0	1	1	0	0	0	0
R15h	Entry mode	0	1	0	0	0	0	0	0	0	0	0	0	0	0	INVDOT	INVDEN	INVHS	INVVS
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(continued)

Reg#	Register	R/W	D/C	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R1Eh	Power control (5)	0	1	0	0	0	0	0	0	0	0	nOTP	0	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0
R22h	RAM data write	0	1	Data[17:0] mapping depends on the interface setting															
	RAM data read	1	1																
R25h	Frame Frequency	0	1	OSC3	OSC2	OSC1	OSC0	0	0	0	0	0	0	0	0	0	0	0	0
	(8000h)			1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R28h	VCOM OTP (000Ah)	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0
R29h	VCOM OTP (80C0h)	0	1	1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0
R30h	γ control (1)	0	1	0	0	0	0	0	PKP12	PKP11	PKP10	0	0	0	0	0	PKP02	PKP01	PKP00
R31h	γ control (2)	0	1	0	0	0	0	0	PKP32	PKP31	PKP30	0	0	0	0	0	PKP22	PKP21	PKP20
R32h	γ control (3)	0	1	0	0	0	0	0	PKP52	PKP51	PKP50	0	0	0	0	0	PKP42	PKP41	PKP40
R33h	γ control (4)	0	1	0	0	0	0	0	PRP12	PRP11	PRP10	0	0	0	0	0	PRP02	PRP01	PRP00
R34h	γ control (5)	0	1	0	0	0	0	0	PKN12	PKN11	PKN10	0	0	0	0	0	PKN02	PKN01	PKN00
R35h	γ control (6)	0	1	0	0	0	0	0	PKN32	PKN31	PKN30	0	0	0	0	0	PKN22	PKN21	PKN20
R36h	γ control (7)	0	1	0	0	0	0	0	PKN52	PKN51	PKN50	0	0	0	0	0	PKN42	PKN41	PKN40
R37h	γ control (8)	0	1	0	0	0	0	0	PRN12	PRN11	PRN10	0	0	0	0	0	PRN02	PRN01	PRN00
R3Ah	γ control (9)	0	1	0	0	0	VRP14	VRP13	VRP12	VRP11	VRP10	0	0	0	0	VRP03	VRP02	VRP01	VRP00
R3Bh	γ control (10)	0	1	0	0	0	VRN14	VRN13	VRN12	VRN11	VRN10	0	0	0	0	VRN03	VRN02	VRN01	VRN00
R41h	Vertical scroll control (1)	0	1	0	0	0	0	0	0	0	VL18	VL17	VL16	VL15	VL14	VL13	VL12	VL11	VL10
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R42h	Vertical scroll control (2)	0	1	0	0	0	0	0	0	0	VL28	VL27	VL26	VL25	VL24	VL23	VL22	VL21	VL20
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R44h	Vertical RAM address position	0	1	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0
	(EF00h)			1	1	1	0	1	1	1	1	0	0	0	0	0	0	0	0
R45h	Horizontal RAM address start position	0	1	0	0	0	0	0	0	0	HSA8	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R46h	Horizontal RAM address end position	0	1	0	0	0	0	0	0	0	HEA8	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0
	(013Fh)			0	0	0	0	0	0	0	1	0	0	1	1	1	1	1	1
R48h	First window start	0	1	0	0	0	0	0	0	0	SS18	SS17	SS16	SS15	SS14	SS13	SS12	SS11	SS10
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R49h	First window end	0	1	0	0	0	0	0	0	0	SE18	SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10
	(00EFh)			0	0	0	0	0	0	0	0	1	1	1	0	1	1	1	1
R4Ah	Second window start	0	1	0	0	0	0	0	0	0	SS28	SS27	SS26	SS25	SS24	SS23	SS22	SS21	SS20
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R4Bh	Second window end	0	1	0	0	0	0	0	0	0	SE28	SE27	SE26	SE25	SE24	SE23	SE22	SE21	SE20
	(00EFh)			0	0	0	0	0	0	0	0	1	1	1	0	1	1	1	1
R4Eh	Set GDDRAM X address counter	0	1	0	0	0	0	0	0	0	0	XAD7	XAD6	XAD5	XAD4	XAD3	XAD2	XAD1	XAD0
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R4Fh	Set GDDRAM Y address counter	0	1	0	0	0	0	0	0	0	YAD8	YAD7	YAD6	YAD5	YAD4	YAD3	YAD2	YAD1	YAD0
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note: In R01h, bits REV, BGR, RL, CM will override the corresponding hardware pins settings.
Setting R28h as 0x0006 is required before setting R25h and R29h registers.

8.2 Initial Code

```
{0x00,0x0001},
 {0x28,0x0006},
 {0x27,0x006D},
 {0x25,0xF000},
 {0x10,0x0000},
 {0x07,0x0033},

 {0x11,0x4270},
 {0x02,0x0600},
 {0x03,0x040E},
 {0x01,0x72EF},
 {0x0F,0x0000},

 {0x0B,0x5308},
 {0x0C,0x0007},
 {0x0D,0x0006},
 {0x0E,0x2D00},
 {0x1E,0x01DD},
 {0x44,0xEF00},
 {0x45,0x0000},
 {0x46,0x013F},
 {0x30,0x0102},
 {0x31,0x0206},
 {0x32,0x0100},
 {0x33,0x0003},
 {0x34,0x0706},
 {0x35,0x0105},
 {0x36,0x0506},
 {0x37,0x0300},
 {0x3A,0x0000},
 {0x3B,0x0000},
```

9 Reliability Test Items

Test Item	Test Conditions	Note
High Temperature Operation	70±3°C , t=240 hrs	
Low Temperature Operation	-20±3°C , t=240 hrs	
High Temperature Storage	80±3°C , t=240 hrs	1,2
Low Temperature Storage	-30±3°C , t=240 hrs	1,2
Storage at High Temperature and Humidity	60°C, 90% RH , 240 hrs	1,2
Thermal Shock Test	-20°C (30min) ~ 70°C (30min) 100 cycles	1,2
Vibration Test (Packing)	Sweep frequency : 10 ~ 55 ~ 10Hz/1min Amplitude : 0.75mm Test direction : X.Y.Z/3 axis Duration : 30min/each axis	2

Note 1 : Condensation of water is not permitted on the module.

Note 2 : The module should be inspected after 1 hour storage in normal conditions (15-35°C , 45-65%RH).

10 USE PRECAUTIONS

10.1 Handling precautions

1) The polarizing plate may break easily so be careful when handling it. Do not touch, press or rub it with a hard-material tool like tweezers.
2) Do not touch the polarizing plate surface with bare hands so as not to make it dirty. If the surface or other related part of the polarizing plate is dirty, soak a soft cotton cloth or chamois leather in benzine and wipe off with it. Do not use chemical liquids such as acetone, toluene and isopropyl alcohol. Failure to do so may bring chemical reaction phenomena and deteriorations.
3) Remove any spit or water immediately. If it is left for hours, the suffered part may deform or decolorize.
4) If the LCD element breaks and any LC stuff leaks, do not suck or lick it. Also if LC stuff is stuck on your skin or clothing, wash thoroughly with soap and water immediately.

10.2 Installing precautions

1) The PCB has many ICs that may be damaged easily by static electricity. To prevent breaking by static electricity from the human body and clothing, earth the human body properly using the high resistance and discharge static electricity during the operation. In this case, however, the resistance value should be approx. 1MΩ and the resistance should be placed near the human body rather than the ground surface. When the indoor space is dry, static electricity may occur easily so be careful. We recommend the indoor space should be kept with humidity of 60% or more. When a soldering iron or other similar tool is used for assembly, be sure to earth it.
2) When installing the module and ICs, do not bend or twist them. Failure to do so may crack LC element and cause circuit failure.
3) To protect LC element, especially polarizing plate, use a transparent protective plate (e.g., acrylic plate, glass etc) for the product case.
4) Do not use an adhesive like a both-side adhesive tape to make LCD surface (polarizing plate) and product case stick together. Failure to do so may cause the polarizing plate to peel off.

10.3 Storage precautions

1) Avoid a high temperature and humidity area. Keep the temperature between 0°C and 35°C and also the humidity under 60%.
2) Choose the dark spaces where the product is not exposed to direct sunlight or fluorescent light.
3) Store the products as they are put in the boxes provided from us or in the same conditions as we recommend.

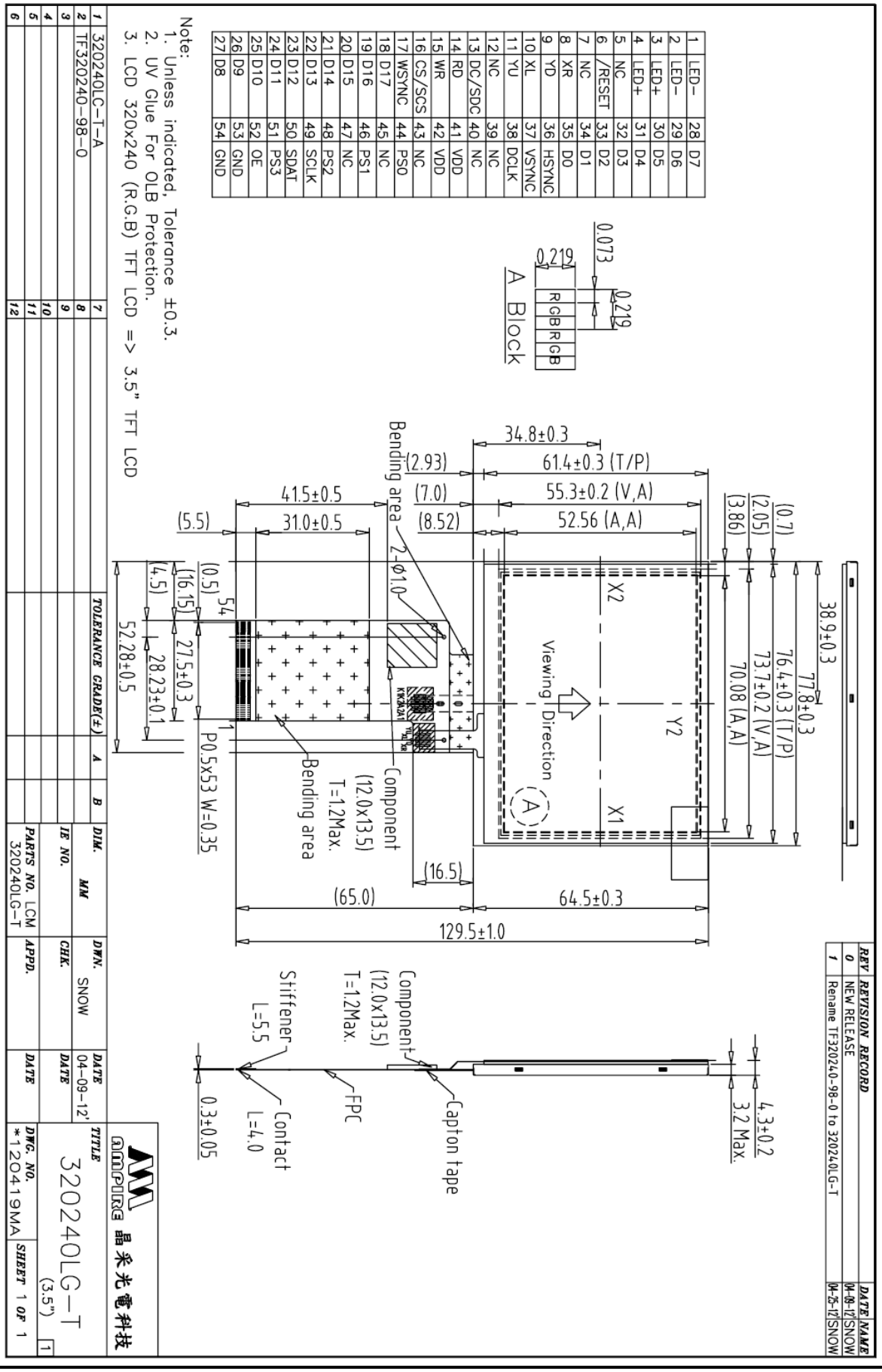
10.4 Operating precautions

1) Do not boost the applied drive voltage abnormally. Failure to do so may break ICs. When applying power voltage, check the electrical features beforehand and be careful. Always turn off the power to the LC module controller before removing or inserting the LC module input connector. If the input connector is removed or inserted while the power is turned on, the LC module internal circuit may break.
2) The display response may be late if the operating temperature is under the normal standard, and the display may be out of order if it is above the normal standard. But this is not a failure; this will be restored if it is within the normal standard.
3) The LCD contrast varies depending on the visual angle, ambient temperature, power voltage etc. Obtain the optimum contrast by adjusting the LC dive voltage.
4) When carrying out the test, do not take the module out of the low-temperature space suddenly. Failure to do so will cause the module condensing, leading to malfunctions.
5) Make certain that each signal noise level is within the standard (L level: 0.2Vdd or less and H level: 0.8Vdd or more) even if the module has functioned properly. If it is beyond the standard, the module may often malfunction. In addition, always connect the module when making noise level measurements.
6) The CMOS ICs are incorporated in the module and the pull-up and pull-down function is not adopted for the input so avoid putting the input signal open while the power is ON.
7) The characteristic of the semiconductor element changes when it is exposed to light emissions, therefore ICs on the LCD may malfunction if they receive light emissions. To prevent these malfunctions, design and assemble ICs so that they are shielded from light emissions.
8) Crosstalk occurs because of characteristics of the LCD. In general, crosstalk occurs when the regularized display is maintained. Also, crosstalk is affected by the LC drive voltage. Design the contents of the display, considering crosstalk.

10.5 Other

1) Do not disassemble or take the LC module into pieces. The LC modules once disassembled or taken into pieces are not the guarantee articles.
2) The residual image may exist if the same display pattern is shown for hours. This residual image, however, disappears when another display pattern is shown or the drive is interrupted and left for a while. But this is not a problem on reliability.
3) AMIPRE will provide one year warrantee for all products and three months warrantee for all repairing products.

11 OUTLINE DIMENSION



1	LED−	28	D7
2	LED−	29	D6
3	LED+	30	D5
4	LED+	31	D4
5	NC	32	D3
6	/RESET	33	D2
7	NC	34	D1
8	XR	35	D0
9	YD	36	HSYNC
10	XL	37	VSYNC
11	YU	38	DCLK
12	NC	39	NC
13	DC/SDC	40	NC
14	RD	41	VDD
15	WR	42	VDD
16	CS/SCS	43	NC
17	WSYNC	44	PS0
18	D17	45	NC
19	D16	46	PS1
20	D15	47	NC
21	D14	48	PS2
22	D13	49	SCLK
23	D12	50	SDAT
24	D11	51	PS3
25	D10	52	OE
26	D9	53	GND
27	D8	54	GND